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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/977,089	UHLER, G. MICHAEL	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-39 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-39 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 12 October 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 37, 38, and 39 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 37, 38, and 39 are directed to an intangible signal because the computer data signal is not contained on a tangible medium.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 4, 5, 6, 7, 27, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 5,371,872 to Larsen et al. ("Larsen"), US

Patent Number 6,332,181 to Bossen et al. ("Bossen"), and US Patent Number 4,056,847 to Marcantonio ("Marcantonio").

5. In reference to Claim 1, Larsen teaches a processing system comprising: a plurality of first interrupts generated by a core (See Column 5 Lines 60-63); a plurality of second interrupts that are generated external to said core (See Column 5 Lines 57-60). Larsen does not teach that said plurality of first interrupts have programmable priorities and a priority encoder, coupled to both said first interrupts and to said second interrupts, said priority encoder prioritizing said first and second pluralities of interrupts utilizing said programmable priorities. Bossen teaches that different priorities can be assigned to different interrupts (See Column 3 Lines 60-61). Marcantonio teaches a priority encoder (See Column 2 Lines 10-15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the interrupt system of Larsen with the programmable priorities of Bossen and the priority encoder of Marcantonio, resulting in the invention of Claim 1, in order to control the handling of simultaneous interrupt requests (See Column 3 Lines 60-62 of Bossen) and to provide a means for producing a signal representative of the highest priority active input (See Column 2 Lines 10-15 of Marcantonio).

6. In reference to Claim 2, Larsen, Bossen, and Marcantonio teach the limits as applied to Claim 1 above. Larsen further teaches that said plurality of first interrupts comprise hardware interrupts and software interrupts (See Column 5 Lines 60-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the interrupt system of Larsen with the programmable priorities of Bossen and the priority encoder of Marcantonio, resulting in the invention of Claim 2, in order to control the handling of simultaneous interrupt requests (See Column 3 Lines 60-62 of Bossen) and to provide a means for producing a signal representative of the highest priority active input (See Column 2 Lines 10-15 of Marcantonio).

7. In reference to Claim 4, Larsen, Bossen, and Marcantonio teach the limits as applied to Claim 1 above. Larsen further teaches that said core executes instructions (See Figure 1 and Column 5 Lines 30-54).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the interrupt system of Larsen with the programmable priorities of Bossen and the priority encoder of Marcantonio, resulting in the invention of Claim 4, in order to control the handling of simultaneous interrupt requests (See Column 3 Lines 60-62 of Bossen) and to provide a means for producing a signal representative of the highest priority active input (See Column 2 Lines 10-15 of Marcantonio).

8. In reference to Claim 5, Larsen, Bossen, and Marcantonio teach the limits as applied to Claim 1 above. Larsen further teaches an interrupt controller, coupled to said plurality of second interrupts, for providing said plurality of second interrupts to said priority encoder with predefined interrupt priorities (See Figure 1 and Column 5 Lines 55-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the interrupt system of Larsen with the programmable priorities of Bossen and the priority encoder of Marcantonio, resulting in the invention of Claim 5, in order to control the handling of simultaneous interrupt requests (See Column 3 Lines 60-62 of Bossen) and to provide a means for producing a signal representative of the highest priority active input (See Column 2 Lines 10-15 of Marcantonio).

9. In reference to Claim 6, Larsen, Bossen, and Marcantonio teach the limits as applied to Claim 1 above. Marcantonio further teaches that said priority encoder produces an indication of which of said first and second pluralities of interrupts has the highest priority (See Column 3 Lines 4-7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the interrupt system of Larsen with the programmable priorities of Bossen and the priority encoder of Marcantonio, resulting in the invention of Claim 6, in order to control the handling of simultaneous interrupt requests (See Column 3 Lines 60-62 of Bossen) and to provide a means for producing a signal representative of the highest priority active input (See Column 2 Lines 10-15 of Marcantonio).

10. In reference to Claim 7, Larsen, Bossen, and Marcantonio teach the limits as applied to Claim 6 above. Marcantonio further teaches a vector generator, coupled to said priority encoder, for receiving said indication, and for producing an interrupt vector corresponding to said interrupt having the highest priority (See Column 3 Lines 38-58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the interrupt system of Larsen with the programmable priorities of Bossen and the priority encoder and vector generator of Marcantonio, resulting in the invention of Claim 7, in order to control the handling of simultaneous interrupt requests (See Column 3 Lines 60-62 of Bossen), to provide a means for producing a signal representative of the highest priority active input (See Column 2 Lines 10-15 of Marcantonio), and to allow selection of the proper interrupt handler for the highest priority interrupt (See Column 3 Lines 47-58 and Column 1 Lines 52-58 of Marcantonio and Column 3 Lines 51-55 of Bossen).

11. In reference to Claim 27, Larsen teaches a method for prioritizing on-core and off-core interrupts within a processing system, comprising: receiving the off-core interrupts (See Column 5 Lines 57-60); and receiving the on-core interrupts (See Column 5 Lines 60-63). Larsen does not teach the on-core interrupts having programmable priority levels; sorting the received off-core and on-core interrupts according to their priority levels; and producing an indication of which of the received off-core and on-core interrupts has the highest priority. Bossen teaches that different priorities can be assigned to different interrupts (See Column 3 Lines 60-61). Marcantonio teaches a priority encoder that can sort the received interrupts according to their priority levels and produces an indication of which of the received interrupts has the highest priority (See Column 2 Lines 10-15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the interrupt method of Larsen with the programmable priorities of Bossen and the priority encoder of Marcantonio, resulting in the invention of Claim 27, in order to control the handling of simultaneous interrupt requests (See Column 3 Lines 60-62 of Bossen) and to provide a method for producing a signal representative of the highest priority active input (See Column 2 Lines 10-15 of Marcantonio).

12. In reference to Claim 29, Larsen, Bossen, and Marcantonio teach the limits as applied to Claim 27 above. Larsen further teaches that the controller decodes received interrupt signals according to well-known priority schemes (See Column 5 Lines 55-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the interrupt method of Larsen with the programmable priorities of Bossen and the priority encoder of Marcantonio, resulting in the invention of Claim 29, in order to control the handling of simultaneous interrupt requests (See Column 3 Lines 60-62 of Bossen) and to provide a method for producing a signal representative of the highest priority active input (See Column 2 Lines 10-15 of Marcantonio).

13. In reference to Claim 30, Larsen, Bossen, and Marcantonio teach the limits as applied to Claim 27 above. The device of Marcantonio inherently examines the priority

levels of the received interrupts. Marcantonio further teaches selecting one of the received interrupts with the highest priority level (See Column 2 Lines 10-15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the interrupt method of Larsen with the programmable priorities of Bossen and the priority encoder of Marcantonio, resulting in the invention of Claim 30, in order to control the handling of simultaneous interrupt requests (See Column 3 Lines 60-62 of Bossen) and to provide a method for producing a signal representative of the highest priority active input (See Column 2 Lines 10-15 of Marcantonio).

14. Claims 3 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen, Bossen, and Marcantonio as applied to Claims 2 and 27 above, and further in view of US Patent Number 5,768,500 to Agrawal et al. ("Agrawal").

15. In reference to Claim 3, Larsen, Bossen, and Marcantonio teach the limitations as applied to Claim 2 above. Larsen further teaches that interrupts can be generated by internal hardware timers (See Column 5 Lines 60-63). Larsen, Bossen, and Marcantonio do not teach that said hardware interrupts comprises a performance counter interrupt. Agrawal teaches the use of a performance counter interrupt (See Column 8 Lines 34-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen, Bossen, and Marcantonio with the

performance counter and interrupt of Agrawal, resulting in the invention of Claim 3, in order to allow development of a cache miss profile by allowing the system to sample the state of the processor at a predetermined number of cache misses as well as to provide assistance in isolating performance bottlenecks and guiding optimization of architectures, operating systems, compilers, and applications (See Column 1 Line 60 – Column 2 Line 6 of Agrawal).

16. In reference to Claim 28, Larsen, Bossen, and Marcantonio teach the limitations as applied to Claim 27 above. Larsen further teaches that interrupts can be generated by internal hardware timers (See Column 5 Lines 60-63). Larsen, Bossen, and Marcantonio do not teach that the on-core interrupts comprise a performance counter interrupt. Agrawal teaches the use of a performance counter interrupt (See Column 8 Lines 34-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen, Bossen, and Marcantonio with the performance counter and interrupt of Agrawal, resulting in the invention of Claim 28, in order to allow development of a cache miss profile by allowing the system to sample the state of the processor at a predetermined number of cache misses as well as to provide assistance in isolating performance bottlenecks and guiding optimization of architectures, operating systems, compilers, and applications (See Column 1 Line 60 – Column 2 Line 6 of Agrawal).

17. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen, Bossen, and Marcantonio as applied to Claim 1 above, and further in view of US Patent Number 5,822,595 to Hu et al. ("Hu").

18. In reference to Claim 8, Larsen, Bossen, and Marcantonio teach the limits as applied to Claim 1 above. Larsen, Bossen, and Marcantonio do not teach a plurality of interrupt priority registers, corresponding to said plurality of first interrupts, said registers for storing said programmable priorities. Hu teaches a plurality of interrupt priority registers for storing the priorities of the interrupt sources (See Abstract and Column 3 Lines 43-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen, Bossen, and Marcantonio with the interrupt priority registers of Hu, resulting in the invention of Claim 8, in order to provide a means to program a priority level to each interrupt source (See Column 3 Lines 41-46 of Hu).

19. In reference to Claim 9, Larsen, Bossen, Marcantonio, and Hu teach the limits as applied to Claim 8 above. Hu further teaches that said plurality of interrupt priority registers are writable by the processing system (See Abstract and Column 3 Lines 43-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen, Bossen, and Marcantonio with the

interrupt priority registers of Hu, resulting in the invention of Claim 9, in order to provide a means to program a priority level to each interrupt source (See Column 3 Lines 41-46 of Hu).

20. Claims 10, 11, 12, 13, 14, 22, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen, Bossen, Marcantonio and Hu.

21. In reference to Claim 10, Larsen teaches a microprocessor for handling interrupts, the microprocessor receiving first interrupts from an interrupt controller (See Column 5 Lines 57-60), the microprocessor comprising a core, for executing instructions, said core generating second interrupts (See Figure 1 and Column 5 Lines 30-54 and 60-63). Larsen does not teach priority storage means coupled to said core, for storing programmable priorities for said second interrupts; and a priority encoder, coupled to said core, and to said priority storage means, for receiving the first and said second interrupts, and for prioritizing the first and said second interrupts utilizing said programmable priorities stored in said priority storage means. Bossen teaches that different priorities can be assigned to different interrupts (See Column 3 Lines 60-61). Marcantonio teaches a priority encoder for prioritizing interrupts (See Column 2 Lines 10-15). Hu teaches a plurality of interrupt priority registers for storing the priorities of the interrupt sources (See Abstract and Column 3 Lines 43-46).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the interrupt system of Larsen with the programmable

priorities of Bossen, the priority encoder of Marcantonio, and interrupt priority registers of Hu, resulting in the invention of Claim 10, in order to control the handling of simultaneous interrupt requests (See Column 3 Lines 60-62 of Bossen), to provide a means for producing a signal representative of the highest priority active input (See Column 2 Lines 10-15 of Marcantonio), and to provide a means to program a priority level to each interrupt source (See Column 3 Lines 41-46 of Hu).

22. In reference to Claim 11, Larsen, Bossen, Marcantonio, and Hu teach the limitations as applied to Claim 10 above. Marcantonio further teaches a priority encoder that receives a plurality of inputs, prioritizes said inputs, and provides said prioritized inputs at an output (See Abstract and Column 2 Lines 5-15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the interrupt system of Larsen with the programmable priorities of Bossen, the priority encoder of Marcantonio, and interrupt priority registers of Hu, resulting in the invention of Claim 11, in order to control the handling of simultaneous interrupt requests (See Column 3 Lines 60-62 of Bossen), to provide a means for producing a signal representative of the highest priority active input (See Column 2 Lines 10-15 of Marcantonio), and to provide a means to program a priority level to each interrupt source (See Column 3 Lines 41-46 of Hu).

23. In reference to Claim 12, Larsen, Bossen, Marcantonio, and Hu teach the limitations as applied to Claim 11 above. Larsen further teaches that the first interrupts

are presented to the microprocessor on first interrupt signal lines attached to the microprocessor (See Figure 1 Number 24).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the interrupt system of Larsen with the programmable priorities of Bossen, the priority encoder of Marcantonio, and interrupt priority registers of Hu, resulting in the invention of Claim 12, in order to control the handling of simultaneous interrupt requests (See Column 3 Lines 60-62 of Bossen), to provide a means for producing a signal representative of the highest priority active input (See Column 2 Lines 10-15 of Marcantonio), and to provide a means to program a priority level to each interrupt source (See Column 3 Lines 41-46 of Hu).

24. In reference to Claim 13, Larsen, Bossen, Marcantonio, and Hu teach the limitations as applied to Claim 10 above. The device of Larsen, Bossen, Marcantonio, and Hu would inherently include code for handling the first interrupts, handling the second interrupts, and storing the programmable priorities into the priority storage means.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the interrupt system of Larsen with the programmable priorities of Bossen, the priority encoder of Marcantonio, and interrupt priority registers of Hu, resulting in the invention of Claim 13, in order to control the handling of simultaneous interrupt requests (See Column 3 Lines 60-62 of Bossen), to provide a means for producing a signal representative of the highest priority active input (See

Column 2 Lines 10-15 of Marcantonio), and to provide a means to program a priority level to each interrupt source (See Column 3 Lines 41-46 of Hu).

25. In reference to Claim 14, Larsen, Bossen, Marcantonio, and Hu teach the limitations as applied to Claim 10 above. Larsen further teaches that said second interrupts generated by said core comprise: hardware interrupts; and software interrupts (See Column 5 Lines 60-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the interrupt system of Larsen with the programmable priorities of Bossen, the priority encoder of Marcantonio, and interrupt priority registers of Hu, resulting in the invention of Claim 14, in order to control the handling of simultaneous interrupt requests (See Column 3 Lines 60-62 of Bossen), to provide a means for producing a signal representative of the highest priority active input (See Column 2 Lines 10-15 of Marcantonio), and to provide a means to program a priority level to each interrupt source (See Column 3 Lines 41-46 of Hu).

26. In reference to Claim 22, Larsen, Bossen, Marcantonio, and Hu teach the limitations as applied to Claim 10 above. Larson further teaches that the interrupt controller prioritizes received interrupt signals according to known priority schemes (See Column 5 Lines 63-65), and therefore the priority encoder uses priorities for the first interrupts established by the interrupt controller when prioritizing the first and second interrupts.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the interrupt system of Larsen with the programmable priorities of Bossen, the priority encoder of Marcantonio, and interrupt priority registers of Hu, resulting in the invention of Claim 22, in order to control the handling of simultaneous interrupt requests (See Column 3 Lines 60-62 of Bossen), to provide a means for producing a signal representative of the highest priority active input (See Column 2 Lines 10-15 of Marcantonio), and to provide a means to program a priority level to each interrupt source (See Column 3 Lines 41-46 of Hu).

27. In reference to Claim 23, Larsen, Bossen, Marcantonio, and Hu teach the limits as applied to Claim 10 above. Marcantonio further teaches that said priority encoder produces an indication of which of said first and second pluralities of interrupts has the highest priority (See Column 3 Lines 4-7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the interrupt system of Larsen with the programmable priorities of Bossen, the priority encoder of Marcantonio, and interrupt priority registers of Hu, resulting in the invention of Claim 23, in order to control the handling of simultaneous interrupt requests (See Column 3 Lines 60-62 of Bossen), to provide a means for producing a signal representative of the highest priority active input (See Column 2 Lines 10-15 of Marcantonio), and to provide a means to program a priority level to each interrupt source (See Column 3 Lines 41-46 of Hu).

28. In reference to Claim 24, Larsen, Bossen, Marcantonio, and Hu teach the limits as applied to Claim 23 above. Marcantonio further teaches a vector generator, coupled to said priority encoder, for receiving said indication, and for producing an interrupt vector corresponding to said interrupt having the highest priority (See Column 3 Lines 38-58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the interrupt system of Larsen with the programmable priorities of Bossen, the priority encoder and vector generator of Marcantonio, and interrupt priority registers of Hu, resulting in the invention of Claim 24, in order to control the handling of simultaneous interrupt requests (See Column 3 Lines 60-62 of Bossen), to provide a means for producing a signal representative of the highest priority active input (See Column 2 Lines 10-15 of Marcantonio), to allow selection of the proper interrupt handler for the highest priority interrupt (See Column 3 Lines 47-58 and Column 1 Lines 52-58 of Marcantonio and Column 3 Lines 51-55 of Bossen), and to provide a means to program a priority level to each interrupt source (See Column 3 Lines 41-46 of Hu).

29. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen, Bossen, Marcantonio, and Hu as applied to Claim 14 above, and further in view of Agrawal.

30. In reference to Claim 15, Larsen, Bossen, Marcantonio, and Hu teach the limitations as applied to Claim 14 above. Larsen further teaches that interrupts can be generated by internal hardware timers (See Column 5 Lines 60-63). Larsen, Bossen, and Marcantonio do not teach that said hardware interrupts comprises a performance counter interrupt. Agrawal teaches the use of a performance counter interrupt (See Column 8 Lines 34-43).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen, Bossen, Marcantonio, and Hu with the performance counter and interrupt of Agrawal, resulting in the invention of Claim 15 , in order to allow development of a cache miss profile by allowing the system to sample the state of the processor at a predetermined number of cache misses as well as to provide assistance in isolating performance bottlenecks and guiding optimization of architectures, operating systems, compilers, and applications (See Column 1 Line 60 – Column 2 Line 6 of Agrawal).

31. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen, Bossen, Marcantonio, and Hu as applied to Claim 10 above, and further in view of US Patent Number 5,664,200 to Barlow et al. ("Barlow").

32. In reference to Claim 16, Larsen, Bossen, Marcantonio, and Hu teach the limitations as applied to Claim 10 above. Larsen, Bossen, Marcantonio, and Hu do not teach that said priority storage means comprises: a plurality of interrupt priority fields,

each of said fields corresponding to one of said second interrupts. Barlow teaches a plurality of registers, each register corresponding to an interrupt, that each contain an interrupt level field (See Figure 2 Number 38 and Column 6 Lines 1-11).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen, Bossen, Marcantonio, and Hu with the pending interrupt registers containing an interrupt priority field of Barlow, resulting in the invention of Claim 16, in order to provide a means to indicate the level of a corresponding interrupt (See Column 6 Lines 5-11 of Barlow).

33. In reference to Claim 17, Larsen, Bossen, Marcantonio, Hu, and Barlow teach the limitations as applied to Claim 16 above. Barlow further teaches that said plurality of interrupt priority fields comprise: a 4-bit field for storing one of sixteen distinct interrupt priorities (See Column 6 Lines 13-15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen, Bossen, Marcantonio, and Hu with the pending interrupt registers containing an interrupt priority field having four bits for identifying 16 interrupt priorities of Barlow, resulting in the invention of Claim 17, in order to provide a means to indicate the level of a corresponding interrupt (See Column 6 Lines 5-11 of Barlow) and provide identification for up to 16 different interrupt levels (See Column 6 Lines 13-15 of Barlow).

34. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen, Bossen, Marcantonio, and Hu as applied to Claim 10 above, and further in view of US Patent Number 5,148,544 to Cutler et al. ("Cutler").

35. In reference to Claim 18, Larsen, Bossen, Marcantonio, and Hu teach the limitations as applied to Claim 10 above. Larsen, Bossen, Marcantonio, and Hu do not teach that said priority storage means is located within a privileged resource within the microprocessor. Cutler teaches that a registers for storing information related to an interrupt condition, is accessible only during a privileged mode (See Abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen, Bossen, Marcantonio, and Hu with the privileged mode register access of Cutler, resulting in the invention of Claim 18, in order to prevent a compromise of the security of other users or programs (See Column 7 Lines 37-40 of Cutler).

36. In reference to Claim 19, Larsen, Bossen, Marcantonio, Hu, and Cutler teach the limitations as applied to Claim 18 above. Cutler further teaches that the privileged mode of operation during which the interrupt registers can be accessed is a kernel mode of operation (See Abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen, Bossen, Marcantonio, and Hu with the privileged (kernel) mode register access of Cutler, resulting in the invention of

Claim 19, in order to prevent a compromise of the security of other users or programs (See Column 7 Lines 37-40 of Cutler).

37. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen, Bossen, Marcantonio, and Hu as applied to Claim 10 above, and further in view of US Patent Number 4,110,822 to Porter et al. ("Porter").

38. In reference to Claim 20, Larsen, Bossen, Marcantonio, and Hu teach the limitations as applied to Claim 10 above. Larsen, Bossen, Marcantonio, and Hu do not teach that the first interrupts have eight distinct priority levels. Porter teaches that interrupts may be assigned to one of eight priority levels (See Column 9 Lines 25-29).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen, Bossen, Marcantonio, and Hu with the interrupt system having eight priority levels of Porter, resulting in the invention of Claim 20, in order to minimize the time required to answer an interrupt request by allowing a complete set of registers to exist for each level, and thus receipt of a higher priority interrupt does not require saving and restoring context data (See Column 9 Lines 25-38 of Porter).

39. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen, Bossen, Marcantonio, Hu, and Porter as applied to Claim 20 above, and further in view of US Patent Number 4,402,042 to Guttag et al. ("Guttag").

40. In reference to Claim 21, Larsen, Bossen, Marcantonio, Hu, and Porter teach the limitations as applied to Claim 20 above. Larsen, Bossen, Marcantonio, Hu, and Porter do not teach that said second interrupts have at least nine distinct priority levels that overlap the priority levels for the first interrupts. Guttag teaches that a processor can have 16 interrupt levels that can be used for internal interrupts (See Column 34 Lines 1-9). Because Guttag and Porter both teach that Interrupt Level 0 is the highest priority and priority levels decrease as interrupt levels increase (See Column 34 Lines 3-4 of Guttag and Column 9 Lines 28-29 of Porter), the interrupt levels of Guttag overlap with the interrupt levels of Porter.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen, Bossen, Marcantonio, Hu, and Porter with the interrupt system having sixteen priority levels of Guttag, resulting in the invention of Claim 21, in order to reserve specific interrupt levels for the different internal interrupts (See Column 34 Lines 5-8 of Guttag).

41. Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen, Bossen, Marcantonio, and Hu as applied to Claim 24 above, and further in view of US Patent Number 5,940,587 to Zimmer ("Zimmer").

42. In reference to Claim 25, Larsen, Bossen, Marcantonio, and Hu teach the limits as applied to Claim 24 above. Larsen, Bossen, Marcantonio, and Hu do not teach

programmable offset storage means, coupled to said vector generator, for providing a programmed offset to said vector generator to allow said vector generator to produce said interrupt vector. Zimmer teaches a programmable offset storage means for providing a programmed offset to said vector generator to allow said vector generator to produce said interrupt vector (See Column 3 Lines 30-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen, Bossen, Marcantonio, and Hu with the programmable offset storage means of Zimmer, resulting in the invention of Claim 25, in order to provide a mechanism for indicating a wide variety of fault conditions without employing multiple default interrupt handler routines by allowing concurrent adjustment of both the segment and the offset without modifying the effective address (See Column 3 Lines 53-59 of Zimmer).

43. In reference to Claim 26, Larsen, Bossen, Marcantonio, and Hu teach the limits as applied to Claim 25 above. Zimmer further teaches that the interrupt vector table containing the offset values is created by a system executive, which is equivalent to kernel mode instructions (See Column 3 Lines 30-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen, Bossen, Marcantonio, and Hu with the programmable offset storage means of Zimmer, resulting in the invention of Claim 26, in order to provide a mechanism for indicating a wide variety of fault conditions without employing multiple default interrupt handler routines by allowing

concurrent adjustment of both the segment and the offset without modifying the effective address (See Column 3 Lines 53-59 of Zimmer).

44. Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen, Bossen, and Marcantonio as applied to Claim 30 above, and further in view of Zimmer.

45. In reference to Claim 31, Larsen, Bossen, and Marcantonio teach the limits as applied to Claim 30 above. Marcantonio further teaches receiving the interrupt with the highest priority level (See Column 3 Lines 4-7). Larsen, Bossen, and Marcantonio do not teach examining a programmable offset; and calculating an interrupt vector for the one of the interrupts with the highest priority level utilizing said programmable offset. Zimmer teaches a programmable offset storage means for providing a programmed offset to said vector generator to allow said vector generator to calculate said interrupt vector (See Column 3 Lines 30-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen, Bossen, and Marcantonio with the programmable offset storage means of Zimmer, resulting in the invention of Claim 31, in order to provide a mechanism for indicating a wide variety of fault conditions without employing multiple default interrupt handler routines by allowing concurrent adjustment of both the segment and the offset without modifying the effective address (See Column 3 Lines 53-59 of Zimmer).

46. In reference to Claim 32, Larsen, Bossen, Marcantonio, and Zimmer teach the limits as applied to Claim 31 above. The device of Zimmer inherently jumps to the interrupt vector in order to access the proper interrupt handler.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen, Bossen, and Marcantonio with the programmable offset storage means of Zimmer, resulting in the invention of Claim 32, in order to provide a mechanism for indicating a wide variety of fault conditions without employing multiple default interrupt handler routines by allowing concurrent adjustment of both the segment and the offset without modifying the effective address (See Column 3 Lines 53-59 of Zimmer).

47. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen, Marcantonio and US Patent Number 5,758,096 to Barsky et al. ("Barsky").

48. In reference to Claim 33, Larsen teaches core generated interrupts (See Column 5 Lines 60-63); and non-core generated inputs (See Column 5 Lines 57-60). Larsen does not teach first program code for providing an interrupt priority encoder for prioritizing between core generated interrupts and non-core generated interrupts; and second program code for providing an interrupt vector generator, for receiving an indication from the priority encoder of a highest priority interrupt, and for generating an interrupt vector for the highest priority interrupt. Marcantonio teaches a priority encoder

capable of prioritizing between two different inputs (See Column 2 Lines 10-15); and a vector generator, for receiving an indication from the priority encoder of a highest priority interrupt, and for generating an interrupt vector for the highest priority interrupt (See Column 3 Lines 38-58). Barsky teaches a computer that uses software to perform a set of method steps (See Column 3 Lines 48-59).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the interrupt system of Larsen with the priority encoder and vector generator of Marcantonio and the computer performing a function using software of Barsky, resulting in the invention of Claim 33, in order to provide a means for producing a signal representative of the highest priority active input (See Column 2 Lines 10-15 of Marcantonio); to allow selection of the proper interrupt handler for the highest priority interrupt (See Column 3 Lines 47-58 and Column 1 Lines 52-58 of Marcantonio) to provide a means for storing the method (See Column 3 Lines 48-59 of Barsky); and because using a computer with software is well-known in the art (See Column 3 Lines 48-51 of Barsky).

49. Claim 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen, Marcantonio and Barsky as applied to Claim 33 above, and further in view of Barlow.

50. In reference to Claim 34, Larsen, Marcantonio, and Barsky teach the limits as applied to Claim 34 above. Larsen, Marcantonio, and Barsky do not teach providing a

plurality of programmable interrupt priority fields that store interrupt priorities associated with the core generated interrupts. Barlow teaches a plurality of registers, each register corresponding to an interrupt, that each contain an interrupt level field (See Figure 2 Number 38 and Column 6 Lines 1-11).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen, Marcantonio, and Barsky with the pending interrupt registers containing an interrupt priority field of Barlow, resulting in the invention of Claim 34, in order to provide a means to indicate the level of a corresponding interrupt (See Column 6 Lines 5-11 of Barlow).

51. In reference to Claim 35, Larsen, Marcantonio, Barsky, and Barlow teach the limits as applied to Claim 34 above. Marcantonio further teaches that the priority encoder is responsive to a plurality of interrupt request signals to indicate the highest priority active interrupt (See Column 2 Lines 10-15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen, Marcantonio, and Barsky with the pending interrupt registers containing an interrupt priority field of Barlow, resulting in the invention of Claim 34, in order to provide a means to indicate the level of a corresponding interrupt (See Column 6 Lines 5-11 of Barlow).

52. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Larsen, Marcantonio and Barsky as applied to Claim 33 above, and further in view of Zimmer.

53. In reference to Claim 36, Larsen, Marcantonio and Barsky teach the limits as applied to Claim 33 above. Larsen, Marcantonio and Barsky do not teach a programmable offset register, the register for storing a memory offset to be used by the interrupt vector generator to calculate the interrupt vector for the highest priority interrupt.. Zimmer teaches a programmable offset register for providing a programmed offset to said vector generator to allow said vector generator to produce said interrupt vector (See Column 3 Lines 30-41).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Larsen, Marcantonio and Barsky with the programmable offset register of Zimmer, resulting in the invention of Claim 36, in order to provide a mechanism for indicating a wide variety of fault conditions without employing multiple default interrupt handler routines by allowing concurrent adjustment of both the segment and the offset without modifying the effective address (See Column 3 Lines 53-59 of Zimmer).

Drawings

54. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Figure 6 Number 608. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are

required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Oath/Declaration

55. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

> The oath or declaration is defective because:
> The specification to which the oath or declaration is directed has not been adequately identified. See MPEP § 601.01(a).

The declaration in the present application refers to a title of "METHOD AND APPARATUS FOR BINDING SHADOW REGISTERS TO VECTORED INTERRUPTS" and a docket number of MIPS:0140.00US. The title of the present application is "CONFIGURABLE PRIORITIZATION OF CORE GENERATED INTERRUPTS" and the docket number is MIPS:0139.00US.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The examiner can normally be reached on Monday-Thursday (7-4:30), Alt. Fridays (7-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tjc

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